Layout Engineer

The IC Layout Engineer is responsible for converting an electrical design to a mask layout used for chip fabrication. He/She is responsible for the physical representation of the chip, from the lowest block level to the complete floor plan. This will be done in close collaboration with the circuit designers and project leaders.

RESPONSIBILITIES / AUTHORITIES:

- Work as a team player in teams of Layout Designers IC Designers.
- Work with engineers in local and international designer teams on the innovative standard cell and pixel layout with the most advanced CIS technologies.
- Responsibilities include all aspects of IC mask design from creating block layout to the complete floor plans; planning schedules, hookup, and verification to tape-out.
- Demonstrates a clear, discipline-specific understanding of the design process.
- Organize to review and work with the circuit designers and peers
- Successfully execute responsibilities in adherence to Qorvo's engineering process.

QUALIFICATIONS:

- Bachelor's Degree in Electrical, Electronic, Telecommunication.
- At least 2 years of proven experience at Layout Designer position and project management.
- Eager and quick to learn in Layout design, verification and work with SoC teams.
- Read and understand detail material specifications and make design / layout decision on these specifications.
- Understanding the physical reason being Design Rule Checks, Layout versus Schematics verification and other physical and electrical design rules will be essential
- Have excellent team-work skill
- Below qualifications are preferred:
    - Good English communication skills in speaking and writting. Have presentation skill in English is a plus
    - Good understanding of Analog/Mixed signal CMOS circuit design concepts is advantage
    - Cadence tools (Virtuoso, LVS/DRC/QRC verification), Unix is desirable