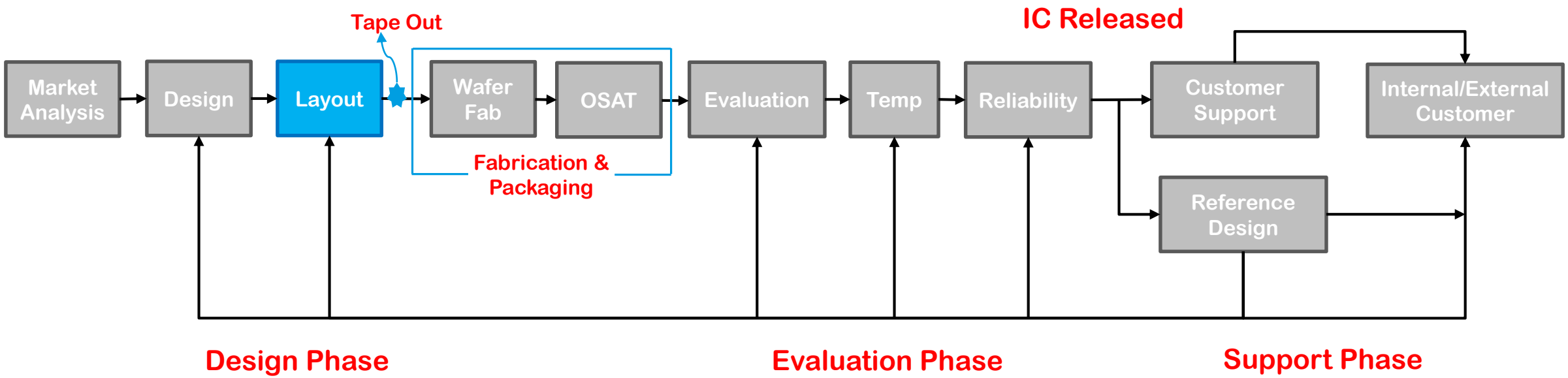
qorvo
all around you

QORVO PROFESSIONAL TRAINING

ANALOG & MIXED-MODE SIGNAL IC LAYOUT DESIGN

Research & Development IC - Full Flow



Design Phase

Mixed Mode Signal Design
**Analog Design Engineer
**Digital Design Engineer
& Customer

Layout Design
****Layout Design Engineer**
**Digital Design Engineer
& Analog Design Engineer

Evaluation Phase

Evaluation
**Application/Firmware Engineer
& Analog Design Engineer
& Digital Design Engineer

Temp - Realiability
**Test Development Engineer
**Production Engineer
& Analog Design Engineer

What does Layout Design Engineer do?

- ✓ Transform circuits diagrams into physical layouts using Cadence Virtuoso Layout Suite, ensure components are accurately placed and connected on the semiconductor chip
- ✓ Optimize circuit layout designs for various parameters like area, power consumption, signal integrity and overall circuit performance
- ✓ Verify layout (LVS, DRC,...) with modern tools to ensure production capacity according to the requirements of the microchip factory.
- ✓ Identify and troubleshooting layout related problems, implement solution to meet design specification & requirement
- ✓ Perform floor-planning so that the microchip can be bonded to the package.
- ✓ Write additional rule-decks to automate the layout optimization process so that the chip achieves the best results, with the fewest unwanted parasitic components.

What you should do to be come a Layout Design Engineer: ***Qorvo professional training course for IC Layout design!***

Fundamental Knowledge:

- ➢ Electronic Circuit Theory
- ➢ Electronic Components

Advanced Knowledge:

❖ Books:
- IC Layout Basics (by Christopher Saint, Judy Saint)
- The Art of Analog Layout (by Alan Hastings)

❖ Tools: Cadence, Mentor Graphics

❖ Forum: https://www.edaboard.com & https://www.edaboard.com/forums/analog-integrated-circuit-ic-design-layout-and.39/

Agenda

1. Objectives & Target Outcomes
2. Training Modules
3. Course Outlines
4. Books & Reference Source

1. Objectives & Target Outcomes

Analog & Mixed-Mode Signal IC Layout Design

OBJECTIVES

✓Training duration: 12 weeks.

✓Integrate theory and practice.

✓Acquire fundamental and essential knowledge of Analog and Mixed-mode signal IC layout design.

✓Gain proficiency in using industry-standard IC layout design tools: Cadence Virtuoso.

✓Learn to adhere to design rules, constraints and specifications in IC layout.

✓Create a portfolio showcasing layout projects and demonstrate proficiency in semiconductor-relevant skills

✓Cultivate a mindset for ongoing learning and staying updated with industry trends and advancement in IC layout design

TARGET OUTCOMES

- Efficient Design Practices: Implement layout designs that optimize area, power and performance metrics for cell and block level.
- Produce Design Tools: Be able to use Cadence Virtuoso Layout Suite L/XL.
- Debug: Develop ability to troubleshoot and debug layout-related issues effectively, capable in using PVS/ Calibre/ Assura to verify layout and fix bugs.
- Cross-functional collaboration: Demonstrate effective communication and collaboration with team members from diverse disciplines
- Documentation Proficiency: Maintain thorough and well-organized documentation for all layout designs.

2. Training Modules

Analog & Mixed-Mode Signal IC Layout Design

IC Fabrication Flow	Components	Device Matching
Introduction analog IC design	MOSFET	Why need matching?
Basic steps of IC fabrication	BJT	Typical matching methods
EDA tool introduction	Resistor	Bi-CMOS matching example
	Capacitor	Resistor matching example
	Diode	Capacitor matching example

2. Training Modules

Analog & Mixed-Mode Signal IC Layout Design

Basic Steps of Layout Design	Verification System	Cadence Tools
Device generation	LVS, ERC	Linux Commands
Floor planning	DRC, ANT	Using Cadence Virtuoso Layout Suite L&XL
Placement		Using PVS/ Assura to check LVS, DRC, ERC, ANT
Routing		Practice layout design of Analog & Mixed-mode signal cell/ block

3. Course Outlines

Analog & Mixed-Mode Signal IC Layout Design

Theory
Practice

Essential Theory	Matching techniques for Layout Design	Device generation, component placement, floor planning and routing	Apply the theoretical knowledge to complete basic block layout	
Component & EDA tools	+ Layout sample of matching	+ Layout sample from circuitry to the completion of physical design using Cadence Virtuoso Layout Suite, Assura/PVS to debug DRC and LVS errors	+ Layout design for basic blocks Current mirrors, Resistor DAC, OTA / Op-amp, Comparator, Oscillator	+ Layout Bandgap Reference Block

WEEK 1-2: FOUNDATION OF IC LAYOUT DESIGN

WEEK 3-4: MATCHING TECHNIQUES IN IC LAYOUT

WEEK 5-6: BASIC STEPS OF LAYOUT DESIGN & VERIFICATION

WEEK 7-8-9-10-11: HANDS ON DESIGN & VERIFICATION

WEEK 12: EXAM & CERTIFICATION

Scope of Knowledge and IC Layout Design Practices

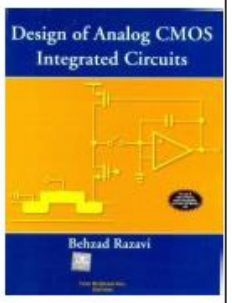
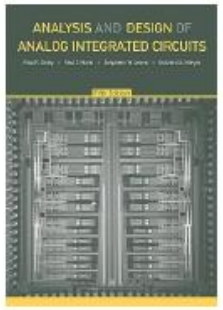
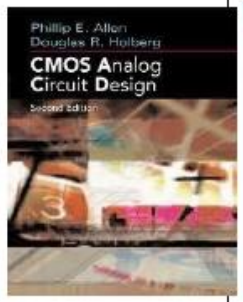
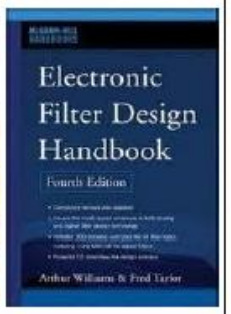
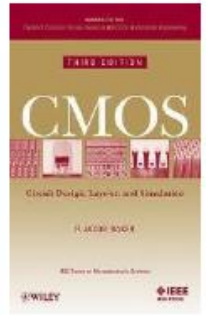
Week	Theory	Hands-on/ Practice
Week 1: Introduction	Basic theory: IC fabrication, introduction analog IC design, EDA tools	
Week 2: Components	• Resistor, Capacitor, CMOS, Diode and Bipolar. • Approaching Cadence Virtuoso Layout Suite L&XL, Cadence PVS/ Assura	▪ Generation device in Cadence Virtuoso Suite L example
Week 3-4: Device Matching	• Why need matching? • Type of matching	▪ Matching Resistor, Capacitor ▪ Matching CMOS and Bipolar
Week 5: Basic steps of layout Design	Component Placement , Floor Planning, and Routing	
Week 6: Layout Verification	• LVS/DRC Verification with Assura/PVS tools	▪ Using Assura/PVS tools to debug errors

Scope of Knowledge and IC Layout Design Practices

Week	Theory	Hands-on/ Practice
Week 7: Block Layout	• Cadence Virtuoso component placement • Resistor matching • NMOS/PMOS matching • BJT matching • Capacitor matching • Floor Planning • Routing • LVS/DRC	▪ Layout Current mirrors
Week 8: Block Layout		▪ Layout Resistor DAC
Week 9: Block Layout		▪ Layout OTA/ Op-Amp
Week 10: Block Layout		▪ Layout Comparator
Week 11: Block Layout		▪ Layout a ring Oscillator
Week 12: Exam & Certification	Hands-on design Bandgap Reference block	

4. Books & Reference Sources

- **The Art of Analog Layout** – *Alan Hastings*
- **IC Layout Basics** – *Christopher Saint/ Judy Saint*
- **IC Mask Design** – *Christopher Saint*
- **Semiconductor Physics and Devices** – *Donald A. Neamen*
- **RF Microelectronics** – *Behzad Razavi*
- **Thiết kế IC Tương Tự** -- *Phạm Nguyễn Thanh Loan*

				
Title: Design of Analog CMOS Integrated Circuits **Author:** Behzad Razavi	**Title:** Analysis and Design of Analog Integrated Circuits **Author:** Gray/ Meyer	**Title:** CMOS Analog Circuit Design **Author:** Phillip Allen	**Title:** Eletronic Filter Design Handbook **Authors:** Williams/ Taylor	**Title:** CMOS circuit Design **Author:** Baker

Thank You